

DX88F01 兼容 8051 指令集 288KBFLASH

DES/TDES ECC SHA-1 USB2.0 ISO7816-3

1. 产品概述

DX88F01 是一款 USB 安全控制芯片，内部集成了 C8051 CPU，288KB Flash 存储空间，4KB XRAM，USB2.0 Full Speed 接口，另有 7816/SPI/I2C/UART 接口，内嵌椭圆曲线 ECC/SHA1/3DES 算法协处理器，集成内部振荡器和 PLL，系统时钟 32MHz，USB 时钟 48MHz，ECC 引擎时钟 96MHz，ECDSA 签名达 18 次/秒，非常适合 USB 安全认证应用。

Part	Interface	CPU	Flash	RAM	Security	Voltage	Package
DX88F01	USB2.0FS	C8051  32MHz	288KB	4KB	ECC/SHA1  3DES/TRNG	2.7-3.6V	QFP48
	7816/SPI						QFN48
	I2C/UART*2						SSOP28

2. 基本特性

CPU

- One clock per machine cycle
- Instruction set compatible with standard 8051
- Four priority levels with 13 interrupt sources
- Three 16-bit Timer/Counter
- 15 bits programmable watchdog timer
- Maximum internal system clock frequency of 32MHz

Memory

- 256 bytes CPU internal data memory (IRAM)
- 4K+256 bytes on-chip external data memory (XRAM),  
therein 256 bytes also can be used for security algorithm engine.
- 288K bytes nonvolatile FLASH memory
  - 4\*64Kbytes/Sector
  - 4\*8KBytes/Sector
  - 96 OTP bytes for FABID, CHIPID and USERID
  - Code and Data memory space freedom configurable
  - Divided into 8 locked/unlocked blocks for code, data,  
algorithm or library locking
  - Software emulation up to 64K bytes EEPROM
  - In-system programmable
  - Single byte program time: 15us
  - Sector erase time: 0.9s
  - Endurance: 100,000@Tj≤1050C

## Security

- Hardware DES and Triple-DES coprocessor
- Mathematical coprocessor for complex operation of large integers
- Maximum 256 bits Elliptic Curves Cryptography (ECC) coprocessor
  - Maximum algorithm engine clock frequency of 96MHz
  - Signature 18 times/second
- Signature Harsh Algorithm (SHA-1)
- Cyclic Redundancy Check (CRC) according to CCIT-16
- Hardware True Random Number Generator according to FIPS140-2
- M-sequence generator for pseudo random number generating
- IRAM, XRAM and FLASH memory address scrambling
- IRAM, XRAM and FLASH memory data encryption
- MOVN and MOVX blocking for accessing no rights sector
- High/Low voltage detection for anti-hacking
- Internal Power On Reset (POR)
- Internal oscillator with In-system trimming
- Unique chip identification number for each chip

## Clock sources

- Integrated PLL clock can be used for USB communication and ECC algorithm acceleration or as system clock
- Internal Oscillator of  $\pm 5\%$  accuracy can be used as PLL reference clock or system clock with SPI, IIC and serial interface communication
- External Oscillator used as PLL reference clock or system clock
- External Clock (XCLK) used as ISO7816 interface communication, PLL reference clock or system clock
- Can switch between clock sources on-the-fly

## Real Time Clock (RTC)

- Full clock feature: second, minute, hour, date, month, and year
- 32.768KHz operation
- Alarm interrupt
- Time tick interrupt

## USB Function

- USB specification 2.0 compliant
- Full speed (12Mbps) operation and integrated transceiver
- Supports 6 endpoints of 1 Control, 2 Bulk In, 2 Bulk Out and 1 Interrupt
- 64 bytes buffer for control endpoint and 8 bytes buffer for interrupt endpoint
- Double-buffers (2\*64 bytes) for each bulk endpoint
- Automatically processing some basic USB protocols in order to

reduce software loading

- Supports remote wake-up

## ISO7816 Function

- ISO7816-3 electrical interface compliant
- Supports ISO7816-3 T=0 and T=1 protocols
- Programmable Baud Rate Generator selects the baud rate as defined in ISO7816-3
- FIFOs for receiver and transmitter
- ISO7816 External clock frequency of 1MHz to 20MHz

## M/S SPI Interface

- Flexible, Full Duplex, Synchronous serial bus
- Operates as Master or Slave device
- Supports multiple masters and slaves on a single SPI bus
- Supports SPI modes 0/1/2/3
- MSB or LSB first data transfer
- Programmable SPI Master clock frequency, maximum up to system clock frequency

## M/S I2C Interface

- Compatible with I2C serial bus standard
- Operates as Master or Slave device
- Start/Stop/Repeated Start generation
- Fully supports arbitration process
- Programmable acknowledge bit, slave device address and master device SCL frequency

## Serial interface

- Serial 0 and Serial 1
- Serial 0 modes 0/1/2/3
- Serial 1 modes 8bits or 9bits
- Serial 0 supports synchronous mode
- Fixed Baud Rate, Timer1 or Internal Baud Rate Generator for serial 0
- Only Internal Baud Rate Generator for Serial 1

## On-Chip Debug

- On-Chip Debug circuit facilitates full speed, non-intrusive in-system debug and in-system programming
- On-Chip 2-wire debug
- Provides breakpoints, step, run, stop, and inspect/modify memory and registers
- Superior performance to emulation system using ICE-chips, target pods and sockets

## GPIO

- Four 8-bits I/O ports
- Each port has each one Pull-up resistor, and can be switched ON or OFF through register configuration
- Each port can be configured four functions: input port, second function port, output port and 3-States in-out port

## Power Management

- Power saving modes IDLE and STOP
- Clocks of function modules can be switched OFF for power saving
- Current consumption < 40mA at 250C with system clock 32MHz, ECC engine clock 96MHz and USB clock 48MHz
- Standby Current consumption < 20uA at 250C with all clocks stop

## Technology

- 0.18um advanced Flash technology
- Operating voltage of 2.7V – 3.6V
- Temperature –400C – 1250C
- ESD protection > 4KV (HBM)

## Development Kits

- Evaluation Board and Emulator
- Keil51 uVision IDE
- Library and Application Notes

## 3. 产品概述

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- e-Banking
- Machine-to-Machine
- e-Payment
- PC Security
- e-Government
- Access Control
- Electronic Transactions Security

## 4. 封装

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- SSOP28
- TQFP48
- QFN48